

11/27/04

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION DISCLOSURE
STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.
200316175-1APPLICATION NO.
10/765,483

CONFIRMATION NO.

APPLICANT

Frederick A. Perner et al.

FILING DATE

herewith

GROUP

2827

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
(P)	1A 6,169,686B1	Jan. 2, 2001	Brug et al.	
	1B 6,259,644B1	Jul. 10, 2001	Tran et al.	
	1C 6,567,297 B2	May 20, 2003	R. Jacob Baker	
	1D 2002/0101758	Aug. 1, 2002	R. Jacob Baker	
(P)	1E 2003/0039162	Feb. 27, 2003	R. Jacob Baker	
	1F			
	1G			
	1H			
	1I			
	1J			
	1K			

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L				
	1M				
	1N				
	1O				
	1P				

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

(P)	1Q	"Nonvolatile RAM based on Magnetic Tunnel Junction Elements" by M. Durlam et al. 2000 IEEE International Solid-State Circuits Conference 07803-5853-8/00, Motorola Labs, Physical Sciences Research Labs, Tempe, AZ, Section TA 7.3
(P)	1R	"A 10ns Read and Write Non-volatile Memory Array Using a Magnetic Tunnel Junction and FET Switch in each Cell" by Roy Scheuerlein et al. 2000 IEEE International Solid-State Circuits Conference 07803-5853-8/00, IBM Research Almaden Research Center, San Jose, CA, Section TA 7.2
(P)	1S	"Offset Compensating Bit-Line Sensing Scheme for High Density DRAM's" by Yohi Watanabe et al., IEE Jurnal of Solid-State Circuits, Vol. 29, No. 1, January 1994.

EXAMINER

See Aubuony

DATE CONSIDERED

6/05